VS2000 Typhoon

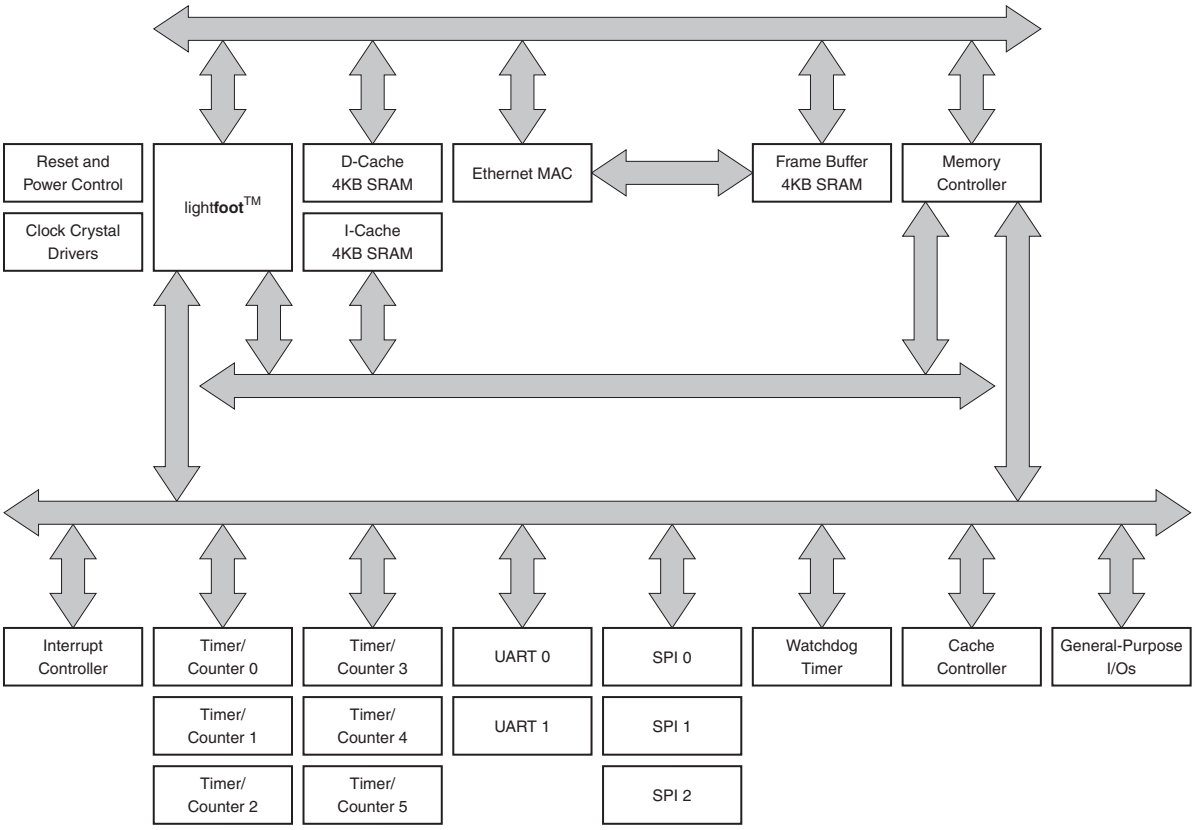
32-Bit Lightfoot™ CPU with Ethernet MAC

Preliminary Datasheet

Features

- Single-supply voltage
  - 3.3V ± 0.3V
- 40 MHz operation (-40°C to +85°C)
  - Derated operation to 50 MHz
- Lightfoot™ core
  - 60 MHz 32-bit processor
  - 4 KB instruction cache
  - 4 KB data cache
- 10/100 Ethernet MAC
  - 3 KB receive buffer
  - 1 KB transmit buffer
- External memory controller
  - 32 MB addressing range
  - 8- or 32-bit external data bus
  - Four programmable chip selects
- Interrupt controller
- Two UARTs
- Three SPI ports
- Watchdog timer
- 87 programmable GPIOs
- Available in 208-lead low-profile PQFP

Block Diagram

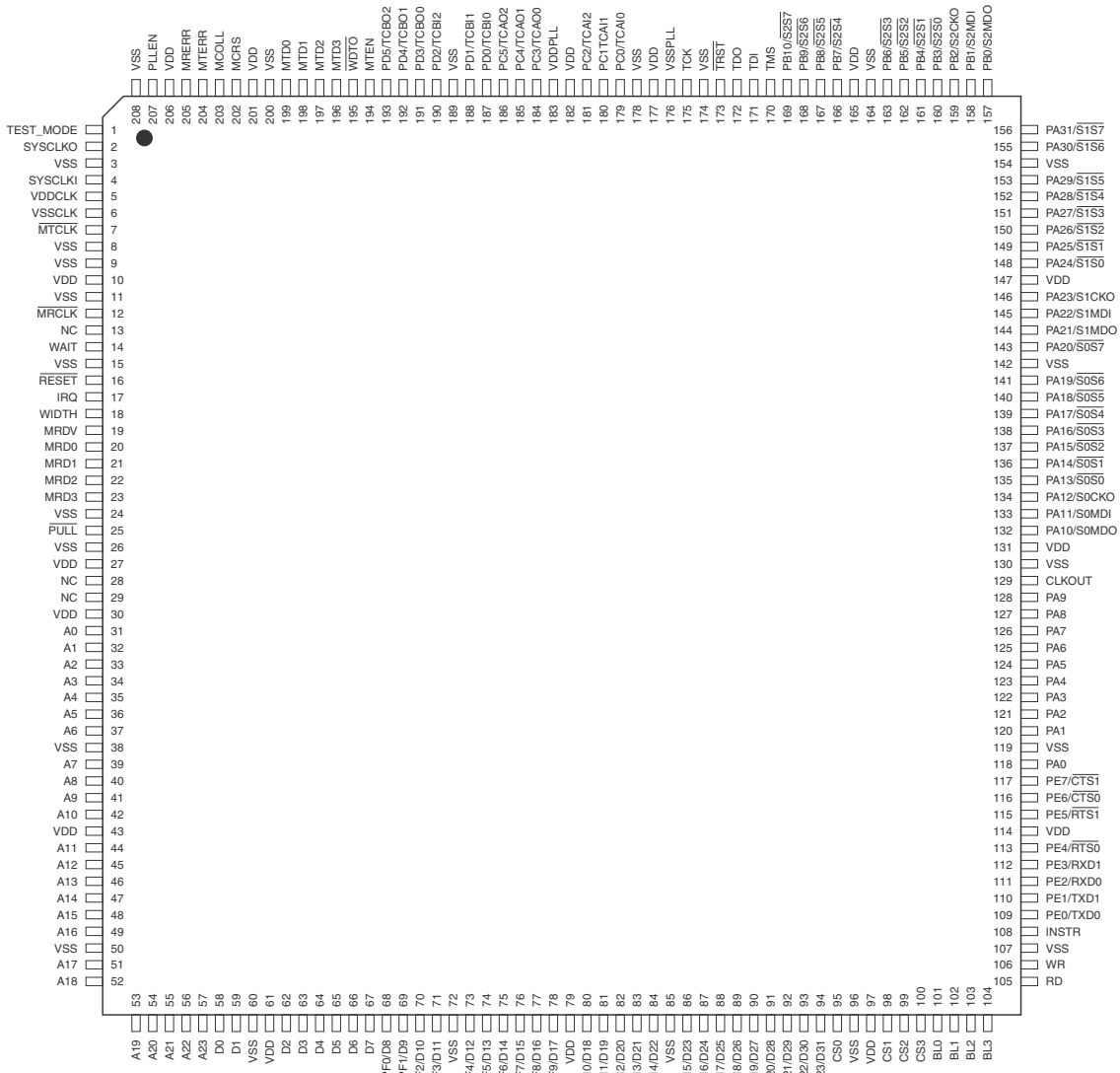


The VS2000, a member of the Typhoon™ family, is a highly-integrated and optimized single-chip network-oriented microcontroller solution. The VS2000 microcontroller incorporates the Lightfoot CPU core, a low-complexity, high-performance 32-bit stack RISC CPU. The Lightfoot CPU makes Typhoon ideal for implementing embedded systems that use object-oriented technologies such as Java™ and .NET™. In addition to the Lightfoot CPU, the Typhoon microcontroller features 4 KB of instruction and data caches, a memory controller with an 8- or 32-bit external interface, an Ethernet MAC unit and a wide range of peripherals including UARTs, timers, GPIOs and SPI in a single-package solution.

The unparalleled code density offered by the Lightfoot architecture and instruction-set offers a dramatic reduction in system memory costs, delivering 32-bit computing at a cost usually associated with 8- and 16-bit solutions. Typhoon is targeted at a wide range of embedded industrial, consumer, networking and machine-to-machine applications.

1.0 Pin Definitions

Figure 1. 208-lead LQFP Pinout Diagram (top view)



1.1 Power Pins

Table 1. Power and Ground

Name	Location	Type	Description
VDDPLL	183	PWR	**PLL Power** — VDDPLL is an isolated power dedicated to Phase Lock Loop (PLL) use. The voltage should be well-regulated and the input should be provided with an extremely low-impedance path to the V_{DD} power rail. VDDPLL should be bypassed to V_{SS} by a 0.47 µF capacitor located as close as possible to the chip package. There is one V_{DDPLL} input.
VDD (15)	10, 27, 30, 43, 61, 79, 97, 114, 131, 147, 165, 177, 182, 201, 206	PWR	**Power** — VDD is the device power supply. These inputs must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are 15 VDD inputs.
VDDCLK	5	PWR	**Clock Power** — VDDCLK is an isolated power dedicated to the clock buffers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one VDDCLK input.
VSSPLL	176	GND	**PLL Ground** — VSSPLL is an isolated ground dedicated to Phase Lock Loop (PLL) use. The connection should be provided with an extremely low impedance path to ground. VSSPLL should be bypassed to V_{SS} by a 0.47 µF capacitor located as close as possible to the chip package. There is one VSSPLL connection.
VSS (24)	3, 8, 9, 11, 15, 24, 26, 38, 50, 60, 72, 85, 96, 107, 119, 130, 142, 154, 164, 174, 178, 189, 200, 208	GND	**Ground** — VSS is the device ground return. This input must be tied externally to all other chip ground inputs. The user must provide adequate external decoupling capacitors. There are 24 VSS inputs.
VSSCLK	6	GND	**Clock Ground** — VSSCLK is an isolated power dedicated to the clock buffers. This input must be tied externally to all other chip ground inputs. The user must provide adequate external decoupling capacitors. There is one VSSCLK input.

1.2 Clock Pins

Table 2. Clocks

Name	Location	Type	Description
SYSCLKI	4	I	**System Clock/Crystal Input** — SYSCLKI interfaces the internal crystal oscillator input to an external crystal or an external clock.
SYSCLKO	2	O	**System Clock/Crystal Output** — SYSCLKO connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave SYSCLKO unconnected.
CLKOUT	129	O	**Clock Output** — CLKOUT provides an output clock synchronized to the internal core clock phase.

1.3 System Control Pins

Table 3. System Control

Name	Location	Type	Description
$\overline{\text{RESET}}$	16	I	**System Reset** — $\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input with pull-up. When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. If the Phase Lock Loop is used, $\overline{\text{RESET}}$ must be asserted for a minimum of 600 µs from power-on. This guarantees that the PLL has locked. If the PLL is not used, $\overline{\text{RESET}}$ must be asserted for a minimum of ten system clock cycles where, in this case, the system clock frequency equals the external clock frequency divided by two. $\overline{\text{RESET}}$ must be asserted after power is applied. $\overline{\text{RESET}}$ is 5V tolerant.
IRQ	17	I	**Interrupt Request** — IRQ is a programmable-edge/level Schmitt-trigger pull-down input maskable interrupt request internally synchronized to CLKOUT. IRQ is 5V tolerant.

1.4 External Memory Interface Pins

Table 4. External Memory Interface

Name	Location	Type	Description
A[23:17] A[16:11] A[10:7] A[6:0]	57-51 49-44 42-39 37-31	O	**Address Bus** — A[23:0] are active-high outputs that specify the address for external program and data memory accesses. To minimize power consumption, A[23:0] do not change state unless external memory spaces are being accessed. The address bus is tri-stated during reset.
D[31:23]/ PF[23:15] D[22:18]/ PF[14:10] D[17:12]/ PF[9:4] D[11:8]/ PF[3:0] D[7:2] D[1:0]	94-86 84-80 78-73 71-68 67-62 59-58	I/O	**Data Bus** — D[31:0] are active-high, bidirectional data bus pins for external program and data memory accesses. The data bus defaults to inputs during reset and are only driven during a write operation. If configured in 8-bit mode, D[7:0] are high-impedance and PF[23:0] are bidirectional GPIO port F. Pins D[31:8] default to GPIO inputs.
CS[3:1] CS0	100-98 95	O	**Chip Select** — CS[3:0] provide four programmable-polarity external chip selects. These signals are tristated during reset.
BL[3:0]	104-101	O	**Byte Lane Select** — BL[3:0] are used to select destination bytes for 32-bit external memory write accesses. These programmable-polarity outputs are tristated during reset.
RD	105	O	**Read Enable** — RD is a programmable-polarity output that is asserted to read external memory on the data bus (D[31:0]). RD is tristated during reset.
WR	106	O	**Write Enable** — WR is a programmable-polarity output that is asserted to write external memory on the data bus (D[31:0]). WR is tristated during reset.
WAIT	14	I	**Wait** — WAIT is an active-high input used by external devices to delay completion of bus cycles. The WAIT input must be asserted synchronously with CLKOUT to guarantee proper operation.
WIDTH	18	I	**Data Bus Width** — The WIDTH input configures the width of the external memory interface. When high the data bus is configured as an 8 bit interface, otherwise the data bus is configured as a 32-bit interface.
INSTR	108	O	**Instruction Access** — INSTR is an active-high output indicating that the current memory access is in the VS2000's program memory space. It is deasserted for external data memory space accesses.

1.5 10/100 PHY MII Pins

Table 5. MII

Name	Location	Type	Description
$\overline{\text{MTCLK}}$	7	I	**Transmit Symbol (nibble) Clock** — $\overline{\text{MTCLK}}$ is supplied by the PHY at 25 MHz for 100 Mbits/sec. operation, at 2.5 MHz for 10 Mbits/sec. $\overline{\text{MTCLK}}$ is a 5V-tolerant pull-down input. MTD[3:0], MTEN and MTERR are synchronous to this clock.
MTD[3:0]	196-199	O	**Transmit Data Nibble** — MTD[3:0] are active-high transmit data nibble outputs. MTD[3:0] are synchronized to the rising edge of MTCLK.
MTEN	194	O	**Transmit Enable** — MTEN is an active-high output that indicates valid data is present on MTD[3:0]. MTEN remains asserted until all nibbles have been clocked into the external PHY. It is deasserted following the clock edge loading the final frame.
MTERR	204	O	**Transmit Coding Error** — MTERR is an active-high output that indicates to the PHY that a coding error has occurred when asserted at the same time as MTEN.
$\overline{\text{MRCLK}}$	12	I	**Receive Symbol (nibble) Clock** — $\overline{\text{MRCLK}}$ is supplied by the PHY at 25 MHz for 100 Mbits/sec. operation, at 2.5 MHz for 10 Mbits/sec. $\overline{\text{MRCLK}}$ is a 5V-tolerant pull-down input.
MRDV	19	I	**Receive Data Valid** — MRDV is an active-high input synchronized to the rising-edge of $\overline{\text{MRCLK}}$. MRDV is asserted by the PHY to indicate that the MRD[3:0] contain valid data. MRDV is a 5V-tolerant pull-down input.
MRD[3:0]	23-20	I	**Receive Data** — MRD[3:0] are active-high receive data nibble inputs. These signals are synchronized to their rising edge of $\overline{\text{MRCLK}}$. MRD[3:0] are 5V-tolerant pull-down inputs.
MRERR	205	I	**Receive Symbol Error** — MRERR is an active-high input signal. It is asserted when a media error is detected by the PHY during transmission of the current frame. MRERR is synchronized with $\overline{\text{MRCLK}}$ and is asserted for one or more clock periods. MRERR is a 5V-tolerant pull-down input.
MCOLL	203	I	**Collision Detected** — MCOLL is an asynchronous active-high input signal indicating that a collision has occurred on the medium. MCOLL is a 5V-tolerant pull-down input.
MCRS	202	I	**Carrier Sense** — MCRS is an asynchronous active-high signal indicating that the medium is in a non-idle state. Otherwise an idle state is indicated (and transmission may start). MCRS is a 5V-tolerant pull-down input.

1.6 UART Pins

Table 6. Serial Communication Interface[1]

Name	Location	Type	Description
TXD0/PE0	109	I/O	**Transmit Data/GPIO** — TXD0 is an active-high UART0 transmit-data output or bidirectional GPIO port E bit 0. RS-232 applications need external RS-232 transmitters to convert voltage levels. This pin defaults to GPIO input.
TXD1/PE1	110	I/O	**Transmit Data/GPIO** — TXD1 is an active-high UART1 transmit-data output or bidirectional GPIO port E bit 1. RS-232 applications need external RS-232 transmitters to convert voltage levels. This pin defaults to GPIO input.
RXD0/PE2	111	I/O	**Receive Data/GPIO** — RXD0 is an active-high UART0 receive-data input or bidirectional GPIO port E bit 2. RS-232 applications need external RS-232 receivers to convert voltage levels. This pin defaults to GPIO input.
RXD1/PE3	112	I/O	**Receive Data/GPIO** — RXD1 is an active-high UART1 receive-data input or bidirectional GPIO port E bit 3. RS-232 applications need external RS-232 receivers to convert voltage levels. This pin defaults to GPIO input.
$\overline{\text{RTS0}}$/PE4	113	I/O	**Request to Send/GPIO** — $\overline{\text{RTS0}}$ is an active-low UART0 flow-control output that indicates the UART is ready to receive data or bidirectional GPIO port E bit 4. RS-232 applications need external RS-232 transmitters to convert voltage levels. This pin defaults to GPIO input.
$\overline{\text{RTS1}}$/PE5	115	I/O	**Request to Send/GPIO** — $\overline{\text{RTS1}}$ is an active-low UART1 flow-control output that indicates the UART is ready to receive data or bidirectional GPIO port E bit 5. RS-232 applications need external RS-232 transmitters to convert voltage levels. This pin defaults to GPIO input.
$\overline{\text{CTS0}}$/PE6	116	I/O	**Clear to Send/GPIO** — $\overline{\text{CTS0}}$ is an active-low UART0 flow-control input that indicates the UART may send data or bidirectional GPIO port E bit 6. RS-232 applications need external RS-232 transmitters to convert voltage levels. This pin defaults to GPIO input.
$\overline{\text{CTS1}}$/PE7	117	I/O	**Clear to Send/GPIO** — $\overline{\text{CTS1}}$ is an active-low UART1 flow-control input that indicates the UART may send data or bidirectional GPIO port E bit 7. RS-232 applications need external RS-232 transmitters to convert voltage levels. This pin defaults to GPIO input.

Note 1. All SCI pins have pull-ups and are not 5V-tolerant.

1.7 Timer Pins

Table 7. Timer/Counter Pins(1)

Name	Location	Type	Description
$\overline{\text{WDTO}}$	195	O	**Watchdog Time-Out** — $\overline{\text{WDTO}}$ is an active-low output that indicates the on-chip watchdog timer has overflowed. This output is active for 16 system clock cycles.
TCAI[2:0]/ PC[2:0] TCBI[1:0]/ PD[1:0] TCBI2/PD2	181-179 188-187 190	I/O	**Timer Counter Input/GPIO** — TCAI0, TCAI1, TCAI2, TCBI0, TCBI1, TCBI2 are programmable-polarity edge-sensitive timer inputs or bidirectional GPIO port C bits 0, 1, 2 and GPIO port D bits 0, 1, 2. These pins have pull-ups and are not 5V-tolerant. These pins default to GPIO inputs.
TCAO[2:0]/ PC[5:3] TCBO[2:0]/ PD[5:3]	186-184 193-191	I/O	**Timer Counter Output/GPIO** — TCAO0, TCAO1, TCAO2, TCBO0, TCBO1, TCBO2 are programmable-polarity timer outputs or bidirectional GPIO port C bits 3, 4, 5 and GPIO port D bits 3, 4, 5. These pins have pull-ups and are not 5V-tolerant. These pins default to GPIO inputs.

Note 1. With the exception of $\overline{\text{WDTO}}$, all timer I/O pins have pull-ups and are not 5V-tolerant.

1.8 GPIO/SPI Pins

Table 8. GPIO Port A/B, SPI2, SPI1, SPI0(1)

Name	Location	Type	Description
PA[31:30]/ $\overline{\text{S1S}}$[7:6] PA[29:24]/ $\overline{\text{S1S}}$[5:0]	156-155 153-148	I/O	**SPI1 Slave Select** — $\overline{\text{S1S}}$[7:0], are active-low output signals used to select the target SPI slave device. **GPIO** — PA[31:24] are general purpose input/output signals. These pins default to GPIO inputs.
PA23/S1CKO	146	I/O	**SPI1 Clock Output** — S1CKO is a programmable SPI clock output. **GPIO** — PA23 is a general purpose input/output signal. This pin defaults to GPIO input.
PA22/S1MDI	145	I/O	**SPI1 Master Data In** — S1MDI is an active-high serial data input for receiving data from SPI slave devices. **GPIO** — PB1 is a general purpose input/output signal. This pin defaults to GPIO input.
PA21/S1MDO	144	I/O	**SPI1 Master Data Out** — S1MDO is an active-high serial output for transmitting data to SPI slave devices. **GPIO** — PB0 is a general purpose input/output signal. This pin defaults to GPIO input.

Note 1. All GPIO and SPI I/O pins have pull-ups and are not 5V-tolerant.

Table 8. GPIO Port A/B, SPI2, SPI1, SPI0[1] (continued)

Name	Location	Type	Description
PA[20]/$\overline{S0S}$[7] PA[19:13]/ $\overline{S0S}$[6:0]	143 141-135	I/O	**SPI0 Slave Select** — $\overline{S0S}$[7:0] are active-low output signals used to select the target SPI slave device. **GPIO** — PA[20:13] are general-purpose input/output signals. These pins default to GPIO inputs.
PA12/S0CKO	134	I/O	**SPI0 Clock Output** — S0CKO is a programmable SPI clock output. **GPIO** — PA12 is a general-purpose input/output signal. This pin defaults to GPIO input.
PA11/S0MDI	133	I/O	**SPI0 Master Data In** — S2MDI is an active-high serial data input for receiving data from SPI slave devices. **GPIO** — PA11 is a general-purpose input/output signal. This pin defaults to GPIO input.
PA10/S0MDO	132	I/O	**SPI0 Master Data Out** — S0MDO is an active-high serial output for transmitting data to SPI slave devices. **GPIO** — PA10 is a general-purpose input/output signal. This pin defaults to GPIO input.
PA[9:1], PA0	128-120, 118	I/O	**GPIO/Interrupt** — PA[9:0] are general-purpose input/output signals. When configured as inputs, bits PA[3:0] can be programmed to function as programmable level-sensitive or edge-sensitive interrupt inputs. When configured as outputs PA[9:0] can drive 12 mA.
PB[10:7]/ $\overline{S2S}$[7:4] PB[6:3]/ $\overline{S2S}$[3:0]	169-166 163-160	I/O	**SPI2 Slave Select** — $\overline{S2S}$[7:0] are active-low output signals used to select the target SPI slave device. **GPIO** — PB[10:3] are general-purpose input/output signals. These pins default to GPIO inputs.
PB2/S2CKO	159	I/O	**SPI2 Clock Output** — S2CKO is a programmable SPI clock output. **GPIO** — PB2 is a general-purpose input/output signal. This pin defaults to GPIO input.
PB1/S2MDI	158	I/O	**SPI2 Master Data In** — S2MDI is an active-high serial data input for receiving data from SPI slave devices. **GPIO** — PB1 is a general-purpose input/output signal. This pin defaults to GPIO input.
PB0/S2MDO	157	I/O	**SPI2 Master Data Out** — S2MDO is an active-high serial output for transmitting data to SPI slave devices. **GPIO** — PB0 is a general-purpose input/output signal. This pin defaults to GPIO input.

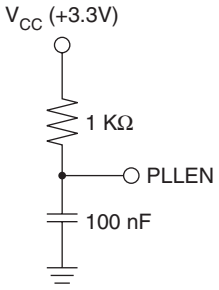
Note 1. All GPIO and SPI I/O pins have pull-ups and are not 5V-tolerant.

1.9 Miscellaneous Pins

Table 9. Miscellaneous

Name	Location	Type	Description
TMS	170	I	**Test Mode Select Input** — Boundary scan input.
TDI	171	I	**Test Data Input** — Boundary scan input.
TDO	172	O	**Test Data Output** — Boundary scan output.
$\overline{\text{TRST}}$	173	I	**Test Reset** — Active-low boundary scan test reset input.
TCK	175	I	**Test Clock Input** — Boundary scan test clock input.
TEST_MODE	1	I	**Device Test Mode Input** — Active-high, 5V-tolerant pull-down production test input. This pin should normally be tied low.
$\overline{\text{PULL}}$	25	I	**Pull-Up/Pull-Down Enable** — Active-low input, enables pull-ups and pull-downs on inputs. This pin is normally tied to V_{SS}, but for power-sensitive applications it may be tied to V_{DD} to disconnect all pull-ups and pull-downs from associated input pins, reducing static power consumption.
PLLEN	207	I	**PLL Enable Input** — Active-high PLL enable Schmitt-trigger input. The PLL may be bypassed by tying this pin low; the system clock frequency will be half the external clock frequency. It is required that PLLEN is low for a minimum of 500 ns following application of power. To accomplish this, using the RC network shown in Figure 2 is suggested.

Figure 2. PLL Enable Input RC Network



2.0 Central Processing Unit

The Lightfoot 32-bit core features a hybrid 8-bit instruction path, 32-bit data path Harvard stack RISC architecture with a unique soft instruction set that allows application specific customization for virtual machine application environments such as Java or .NET. The memory referenced by programs falls into two categories: instruction memory and data memory. Instruction memory is eight bits wide and is used to store program instructions and constant data. Data memory is 32 bits wide and is byte addressable. Words (32-bit quantities) must be word-aligned, half-words (16-bit quantities) must be half-word aligned. The memory interface detects illegal accesses and signals a Bus Error trap.

The instruction and data memory interfaces each use 24-bit addresses allowing a total of 32 MB of off-core memory to be addressed. In addition to these interfaces, the Lightfoot core also features a 256 word, single-cycle 32-bit register interface that is used to access on-chip peripheral and core resources. The register port uses 8-bit addresses.

The Lightfoot core provides the following functional blocks:

- Control Unit
- ALU
- Data and Return Stacks
- Core Registers

2.1 Control Unit

The Control Unit is responsible for fetching, decoding and sequencing the execution of instructions in the processor. It also contains modules for implementing run-time checks and trap handling.

2.2 Arithmetic and Logic Unit

The ALU performs all the arithmetic and logical operations on data operands present in the data stack. The 32-bit ALU features a multi-cycle 32-bit barrel shifter and a 2-bit multiply step unit (allowing a 32 x 32-bit multiply to execute in 16 cycles) in addition to the usual arithmetic and logic capabilities.

2.3 Data And Return Stacks

The Data Stack plays the role of a register bank in traditional architectures. It consists of a hardware part (implemented as a bank of eight 32-bit core registers) and a memory extension unit. The memory extension unit is supported by a dedicated register (the EP, or Extension Pointer) together with a fill/spill circuit. The data stack is used to hold temporary data; it is not used to implement the stack frame for which special support is provided. The top elements of the Data Stack are coupled to the inputs of the ALU.

The Return Stack plays a threefold role in the processor: it holds return addresses for subroutines, its top-of-stack element is used as an index register to access program memory, and it can be used as an auxiliary stack for programs. The organization of the Return Stack is similar to the organization of the Data Stack, in that it also consists of a hardware part and a memory extension unit. The hardware part of the Return Stack consists of four 32-bit registers. The memory extension unit is supported by a dedicated CPU register (called the REP, Return Extension Pointer) and a fill/spill circuit.

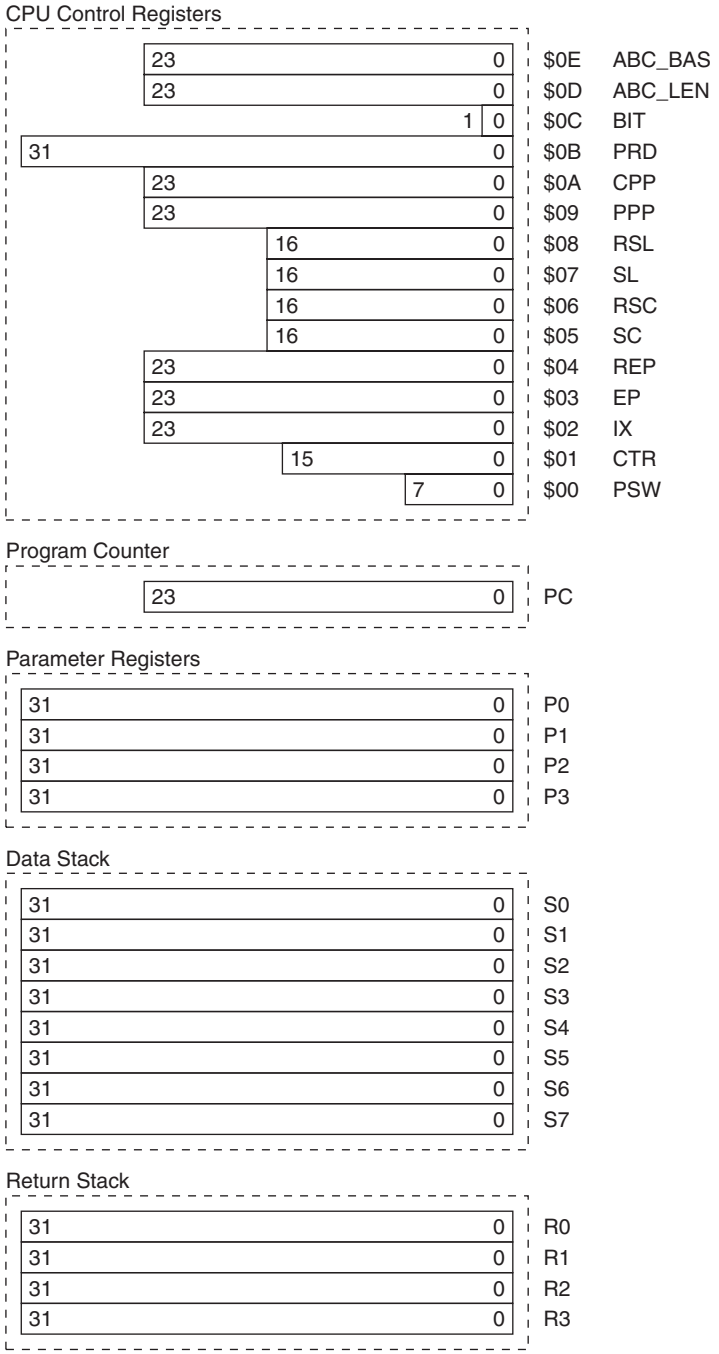
2.4 Core Registers

Core registers fall into two categories, those that can be read or written via the 256-word register bus and those that can not. The bottom 32 address slots are reserved for core use, the remainder are available for

interfacing to system peripherals such as memory management units or cryptographic co-processors. Of the 32 reserved slots, 15 are currently used as indicated in the figure below.

Address pointer registers: IX, EP, REP, CPP and PPP are always word-aligned, i.e. the two LSBs are always set to zero.

Figure 3. Lightfoot Programming Model



3.0 Other Functional Blocks

3.1 Cache Units

The VS2000 has internal instruction and data caches, each of 4K bytes. To raise the cache-hit ratio, the cache is configured using two-way, set-associative addressing. The replacement algorithm is LRU (Least Recently Used). Each set uses a 12-bit tag address. The cache line size is four words (16 bytes). Valid, dirty and lock bits indicate the status of each cache line. The valid bit indicates the associated line has valid data, the dirty bit indicates that the line contains data that needs to be written to main memory and the lock bit indicates that the line cannot be replaced. When a miss occurs, four words must be fetched consecutively from external memory. Typically, RISC processors take advantage of instruction/data caches to improve performance. Without an instruction cache, bottlenecks that occur during instruction fetches from external memory may seriously degrade performance.

3.2 10/100 Ethernet MAC with DMA

The VS2000 has an Ethernet controller that operates at either 100 Mbits or 10 Mbits per second in half-duplex or full-duplex mode. The MII supplies the transmit and receive clocks of 25 MHz for 100 Mbits/second operation or 2.5 MHz at the 10 Mbits/second speed. An integrated DMA controller transfers data between the MII interface and frame buffers. The Ethernet MAC memory system contains a 1 KB transmit buffer and a 3 KB receive buffer. An external PHY is needed for the complete Ethernet solution.

3.3 Memory Controller

The memory controller generates the signals that control the access to external memory or peripheral devices. The unit is programmable and can address up to 32 MB of off-chip unified instruction/data memory. It has four chip selects and a 24-bit address bus. The external data bus can be configured to interface with 8- or 32-bit external devices. Separate read and write control signals allow for direct memory and peripheral interfacing.

3.4 Interrupt Controller

The VS2000 has a 16-level priority, individually-maskable, vectored interrupt controller. This feature substantially reduces the software and real-time overhead in handling internal and external interrupts. The 16-level priority encoder allows the customer to define the priority between the different interrupt sources. Internal sources are programmed to be level sensitive or edge triggered. External sources can be programmed to be positive- or negative-edge triggered or high- or low-level sensitive.

3.5 UARTs

The VS2000 provides two identical, full-duplex, universal synchronous/asynchronous receiver/transmitters that support standard features such as parity, framing and overrun error detection, line break generation and detection, interrupt generation and flow control. Each UART also includes a programmable baud-rate generator.

3.6 SPI Ports

The VS2000 provides three identical master-only SPI-compatible serial communication ports that directly supports a number of SPI operational features such as programmable frame transfer length, clock rate, clock polarity and clock phase. SPI slave devices typically include D/A and A/D converters, UARTs, memories and sensors. Each SPI port supports the direct connection of up to eight SPI slave devices.

3.7 Timers

The VS2000 features two timer/counter blocks, each containing three identical 32-bit timer/counter channels. Each channel can be independently programmed to perform a wide range of functions including event counting, interval measurement, pulse generation, delay timing and pulse width modulation. Each timer/counter channel has three external clock inputs, five internal clock inputs, and two multi-purpose input/output signals that can be configured by the user. Each channel drives an internal interrupt signal that can be programmed to generate processor interrupts via the interrupt controller.

3.8 Watchdog Timer

The Typhoon series microcontrollers have an internal watchdog timer that can be used to prevent system lock-up if the software becomes trapped in a deadlock. In normal operation the user reloads the watchdog at regular intervals before the timer timeout condition occurs. A watchdog timeout condition occurs when the watchdog control register has not been written to within a programmable timeout period. When a timeout condition occurs, the watchdog timeout signal is driven low for a duration of 16 system clock cycles. This output can be used by other devices within the system to reset or respond in an appropriate manner.

3.9 General-Purpose I/Os

The VS2000 has 87 programmable I/O lines. Each of the I/O lines is multiplexed with an external signal of a peripheral to optimize the use of available package pins. Six separate GPIO controllers control these lines. Eight of the GPIO pins also provide an external internal interrupt signal to the interrupt controller; the interrupt signals can be programmed as edge sensitive or level sensitive.

4.0 Instruction Set

The Lightfoot instruction set has been designed to allow highly-efficient execution of programs developed using object-oriented technologies such as Java, .NET, while still remaining highly flexible through the Lightfoot soft byte code mechanism.

The opcode field of a Lightfoot instruction is always eight bits wide; having three instruction formats which are:

- Soft Byte Code
- Fast Return
- Non-Returnable

A total of 128 of the possible 256 Lightfoot instructions are fixed instructions. These instructions comprise all Fast-Return and Non-Returnable instructions. The remaining 128 of the 256 possible Lightfoot instruction codes are user-configurable. These instructions are known as soft byte codes. Soft byte codes deliver the time efficiency of in-line code without sacrificing code density, making the processor ideal for creating efficient virtual machines (to support technologies such as Java), legacy instruction set emulation (8051) and application-specific instructions (for encryption support).

A number of Lightfoot instructions use operands which immediately follow the instruction opcode. These operands may be either eight or 16 bits wide, signed or unsigned.

4.1 Fast Return Instructions

A subset of 32 of the 128 fixed Lightfoot instructions which are single byte-only instructions (they do not require immediate data) and have Fast Return variants. Fast Return instructions permit zero overhead return from subroutines to be folded with their execution.

During the cycle after a Fast Return instruction is fetched from program memory, the Program counter takes on the value from the top of the Return Stack (RS0).

4.2 Non-Returnable Instructions

A subset of 64 of the 128 hard-coded Lightfoot instructions are non-returnable, i.e. their execution may not be folded with a subroutine return. These non-returnable instructions typically have immediate data or use the Return Stack during their execution.

4.3 Instruction Prefixes

A number of instructions may be prefixed with either WIDE or UNSGN instruction opcodes. These prefix opcodes alter how the instruction is executed by Lightfoot. The following subsections describe each of these prefix instruction opcodes.

4.3.1 WIDE Instruction

If an instruction, which uses an immediate operand is prefixed by the WIDE opcode, the immediate operand is taken to be 16 bits wide, with the most significant eight bits coming first followed by the least significant eight bits (big endian ordering). The resulting 16-bit value is interpreted as a signed or unsigned value, depending on the particular instruction.

4.3.2 UNSGN (Unsigned) Instruction

A number of instructions which normally use signed data in their execution may be forced to use unsigned data by prefixing their opcode (or associated WIDE opcode) with an UNSGN (unsigned) opcode.

There are three types of instruction which may use the UNSGN opcode, these include data memory byte and half-word loads, program memory immediate constant loads and branch condition comparisons which compare the top two Data Stack elements. The following summarizes the use of the UNSGN opcode with each of these instruction types:

- In the case of unsigned byte and half-word data memory loads, an UNSGN instruction prefix will prevent sign extension of the data loaded onto the top Data Stack as a result of the instruction execution. Instead, the data loaded onto the top Data Stack element is zero extended.
- In the case of unsigned program memory immediate constant loads, an UNSGN instruction prefix will prevent sign extension of constant data loaded onto the Data Stack. Instead, the data loaded onto the top Data Stack element is zero extended.
- In the case of branch condition comparisons, an UNSGN instruction prefix will force top two stack elements to be treated as 32-bit unsigned numbers. The branch offset values are not affected by the UNSGN instruction (they remain signed).

4.3.2.1 Instruction Byte Sequences

Lightfoot instructions (assuming that WIDE and UNSGN are part of an instruction) can thus be 8, 16, 24, 32 or 40 bits wide.

4.3.2.2 Instruction Set Summary

Table 10. Arithmetic and Logical Instructions

Mnemonic	Description	Mnemonic	Description
ADD	Add	ASR	Arithmetic shift right
ADC	Add with carry	ROT	Rotate left
AND	Bitwise AND	MUL	Multiplication step
IOR	Bitwise inclusive OR	NEG	Negate
XOR	Bitwise exclusive OR	CPL	One's complement
SUB	Subtract	INC	Increment
SBC	Subtract with carry	DEC	Decrement
SHL	Shift left	SEXB	Sign-extend byte
SHR	Shift right	SEXH	Sign-extend half-word

Table 11. Stack Manipulation Instructions

Mnemonic	Description	Mnemonic	Description
POP	Drop top data stack element	RROT	Right rotate top three data stack elements
DUP	Copy top data stack element	TOVER	Copy third data stack element to top
OVER	Copy second data stack element to top	RPOP	Move top return stack element to data stack
SWAP	Swap top two data stack elements	RPUSH	Move top data stack element to return stack
LROT	Left rotate top three data stack elements		

Table 12. Constant, Local Variable, Register and Parameter Register Instructions

Mnemonic	Description	Mnemonic	Description
CNSTI	Immediate constant	LP2	Load P2
CNST	Constant	LP3	Load P3
LP	Load parameter	SP0	Store P0
SP	Store parameter	SP1	Store P1
LPAR	Load parameter (direct)	SP2	Store P2
SPAR	Store parameter (direct)	SP3	Store P3
LPA	Load parameter address	LR	Load register
LP0	Load P0	SR	Store register
LP1	Load P1		

Table 13. Program and Data Memory Access Instructions

Mnemonic	Description	Mnemonic	Description
LIP	Load indexed program memory	LXB	Load indexed byte
SIP	Store indexed program memory	SXB	Store indexed byte
LW	Load word	LOW	Load offset word
SW	Store word	SOW	Store offset word
LH	Load half-word	LOH	Load offset half-word
SH	Store half-word	SOH	Store offset half-word
LB	Load byte	LOB	Load offset byte
SB	Store byte	SOB	Store offset byte
LWIX	Load word via index register	LDW	Load direct word
SWIX	Store word via index register	SDW	Store direct word
LXW	Load indexed word	LDH	Load direct half-word
SXW	Store indexed word	SDH	Store direct half-word
LXH	Load indexed half-word	LDB	Load direct byte
SXH	Store indexed half-word	SDB	Store direct byte

Table 14. Control Flow Instructions

Mnemonic	Description	Mnemonic	Description
DBNZ	Loop while counter register is greater than zero	BGEZ	Branch on greater than or equal to zero
BR	Unconditional branch	BLEZ	Branch on less than or equal to zero
JMP	Jump	BEQ	Branch on equal
BSR	Branch to subroutine	BNE	Branch on not equal
JSR	Jump to subroutine	BGT	Branch on greater than
BZ	Branch on zero	BLT	Branch on less than
BNZ	Branch on not zero	BGE	Branch on greater than or equal to
BGZ	Branch on greater than zero	BLE	Branch on less than or equal to
BLZ	Branch on less than zero		

Table 15. Stack Frame Support and Other Instructions

Mnemonic	Description	Mnemonic	Description
SSF	Set up stack frame	USGN	Unsigned prefix
PARS	Parameter store	WIDE	Wide prefix
REGS	Register store	NOP	No operation (return)

5.0 Memory Maps

Typhoon has three memory areas: instruction memory, data memory and register port. The Ethernet MAC unit is configured using the data memory interface, all other peripherals are configured using the register port.

Table 16. Register Port Memory Map

Register Port Address	Register Name	Width (bits)	Description	Reset Value
$00	PSW	8	Processor status word register, in-core	$00
$01	CTR	16	Counter register, in-core	$0000
$02	IX	24	Index register, in-core	$000000
$03	EP	24	Data stack extension pointer register, in-core	$000000
$04	REP	24	Return stack extension pointer register, in-core	$000000
$05	SC	17	Stack counter register, in-core	$1FFFC
$06	RSC	17	Return stack counter register, in-core	$1FFFF
$07	SL	17	Data stack limit register, in-core	$1FFFC
$08	RSL	17	Return stack limit register, in-core	$1FFFF
$09	PPP	24	Parameter pool pointer register, in-core	$000000
$0A	CPP	24	Constant pool pointer register, in-core	$000000
$0B	PRD	32	Product register, in-core	$00000000
$0C	BIT	2	Bit register, in-core	$000000
$0D	ABC_LEN	16	Array bounds check length register, in-core	$0000
$0E	ABC_BAS	24	Array bounds check base register, in-core	$000000
$0F-$1F	Reserved	n/a	Reserved for future in-core expansion	n/a
$20	TACSR0	8	Triple timer module A, timer 0 write command, read status register	$00
$21	TAMR0	4	Triple timer module A, timer 0 mode register	$0

Note 1. Undefined at power-up, unmodified by reset.
2. Bits 11-0 are undefined, unmodfied by reset.

Table 16. Register Port Memory Map (continued)

Register Port Address	Register Name	Width (bits)	Description	Reset Value
$22	TAIOR0	4	Triple timer module A, timer 0 IO register	$4
$23	TACVR0	32	Triple timer module A, timer 0 count value register	$00000000
$24	TAPLR0	32	Triple timer module A, timer 0 pre-load register	$00000000
$25	TAMCVR0	32	Triple timer module A, timer 0 middle count value register	$FFFFFF00
$26	TAECVR0	32	Triple timer module A, timer 0 end count value register	$FFFFFFFF
$27	TAMVR0	32	Triple timer module A, timer 0 measurement value register	$00000000
$28	TACSR1	32	Triple timer module A, timer 1 write command, read status register	$00
$29	TAMR1	32	Triple timer module A, timer 1 mode register	$0
$2A	TAIOR1	32	Triple timer module A, timer 1 IO register	$4
$2B	TACVR1	32	Triple timer module A, timer 1 count value register	$00000000
$2C	TAPLR1	32	Triple timer module A, timer 1 pre-load register	$00000000
$2D	TAMCVR1	32	Triple timer module A, timer 1 middle count value register	$FFFFFF00
$2E	TAECVR1	32	Triple timer module A, timer 1 end count value register	$FFFFFFFF
$2F	TAMVR1	32	Triple timer module A, timer 1 measurement value register	$00000000
$30	TACSR2	8	Triple timer module A, timer 2 write command, read status register	$00
$31	TAMR2	4	Triple timer module A, timer 2 mode register	$0
$32	TAIOR2	4	Triple timer module A, timer 2 IO register	$4
$33	TACVR2	32	Triple timer module A, timer 2 count value register	$00000000
$34	TAPLR2	32	Triple timer module A, timer 2 pre-load register	$00000000
$35	TAMCVR2	32	Triple timer module A, timer 2 middle count value register	$FFFFFF00
$36	TAECVR2	32	Triple timer module A, timer 2 end count value register	$FFFFFFFF

Note 1. Undefined at power-up, unmodified by reset.

2. Bits 11-0 are undefined, unmodfied by reset.

Table 16. Register Port Memory Map (continued)

Register Port Address	Register Name	Width (bits)	Description	Reset Value
$37	TAMVR2	32	Triple timer module A, timer 2 measurement value register	$00000000
$38-$3E	Reserved	n/a	Reserved	n/a
$3F	TAISR	3	Triple timer module A interrupt status register	$0
$40	TBCSR0	8	Triple timer module B, timer 0 write command, read status register	$00
$41	TBMR0	4	Triple timer module B, timer 0 mode register	$0
$42	TBIOR0	4	Triple timer module B, timer 0 IO register	$4
$43	TBCVR0	32	Triple timer module B, timer 0 count value register	$00000000
$44	TBPLR0	32	Triple timer module B, timer 0 pre-load register	$00000000
$45	TBMCVR0	32	Triple timer module B, timer 0 middle count value register	$FFFFFF00
$46	TBECVR0	32	Triple timer module B, timer 0 end count value register	$FFFFFFFF
$47	TBMVR0	32	Triple timer module B, timer 0 measurement value register	$00000000
$48	TBCSR1	8	Triple timer module B, timer 1 write command, read status register	$00
$49	TBMR1	4	Triple timer module B, timer 1 mode register	$0
$4A	TBIOR1	4	Triple timer module B, timer 1 IO register	$4
$4B	TBCVR1	32	Triple timer module B, timer 1 count value register	$00000000
$4C	TBPLR1	32	Triple timer module B, timer 1 pre-load register	$00000000
$4D	TBMCVR1	32	Triple timer module B, timer 1 middle count value register	$FFFFFF00
$4E	TBECVR1	32	Triple timer module B, timer 1 end count value register	$FFFFFFFF
$4F	TBMVR1	32	Triple timer module B, timer 1 measurement value register	$00000000
$50	TBCSR2	8	Triple timer module B, timer 2 write command, read status register	$00
$51	TBMR2	4	Triple timer module B, timer 2 mode register	$0
$52	TBIOR2	4	Triple timer module B, timer 2 IO register	$4

Note 1. Undefined at power-up, unmodified by reset.

2. Bits 11-0 are undefined, unmodfied by reset.

Table 16. Register Port Memory Map (continued)

Register Port Address	Register Name	Width (bits)	Description	Reset Value
$53	TBCVR2	32	Triple timer module B, timer 2 count value register	$00000000
$54	TBPLR2	32	Triple timer module B, timer 2 pre-load register	$00000000
$55	TBMCVR2	32	Triple timer module B, timer 2 middle count value register	$FFFFFF00
$56	TBECVR2	32	Triple timer module B, timer 2 end count value register	$FFFFFFFF
$57	TBMVR2	32	Triple timer module B, timer 2 measurement value register	$00000000
$58-$5E	Reserved	n/a	Reserved	n/a
$5F	TBISR	3	Triple timer module B interrupt status register	$0
$60-$6F	Reserved	n/a	Reserved	n/a
$70	ICCSR	32	Instruction cache write control/read status register	$00800xxx(2)
$71	DCCSR	32	Data cache write control/read status register	$00800xxx(2)
$72	WDTCSR	8	Watchdog timer write command/read status register	$80
$73	WDTCR	32	Watchdog timer count value register	$00000000
$74	Reserved	n/a	Reserved	n/a
$75	Reserved	n/a	Reserved	n/a
$76	Reserved	n/a	Reserved	n/a
$77	Reserved	n/a	Reserved	n/a
$78	PACR	32	Port A I/O configuration register	$00000000
$79	PBCR	11	Port B I/O configuration register	$000
$7A	PCCR	6	Port C I/O configuration register	$00
$7B	PDCR	6	Port D I/O configuration register	$00
$7C	PECR	8	Port E I/O configuration register	$00
$7D	PFCR	24	Port F I/O configuration register	$000000
$7E-$7F	Reserved	n/a	Reserved	n/a
$80	UDR0	8	UART0 write transmit/read receive data register or divisor low	$00
$81	UIER0	8	UART0 interrupt enable register or divisor high	$00

Note 1. Undefined at power-up, unmodified by reset.

2. Bits 11-0 are undefined, unmodfied by reset.

Table 16. Register Port Memory Map (continued)

Register Port Address	Register Name	Width (bits)	Description	Reset Value
$82	UIIR0	8	UART0 write FIFO control/read interrupt identification register	$C1
$83	ULCR0	8	UART0 line control register	$03
$84	UMCR0	8	UART0 modem control register	$00
$85	ULSR0	8	UART0 line status register	$60
$86	UMSR0	8	UART0 modem status register	$00
$87	Reserved	n/a	Reserved	n/a
$88	UDR1	8	UART1 write transmit/read receive data register or divisor low	$00
$89	UIER1	8	UART1 interrupt enable register or divisor high	$00
$8A	UIIR1	8	UART1 write FIFO control/read interrupt identification register	$C1
$8B	ULCR1	8	UART1 line control register	$03
$8C	UMCR1	8	UART1 modem control register	$00
$8D	ULSR1	8	UART1 line status register	$60
$8E	UMSR1	8	UART1 modem status register	$00
$8F-$9F	Reserved	n/a	Reserved	n/a
$A0	PADR	32	Port A data register	$00000000
$A1	PADDR	32	Port A data direction register	$FFFFFFFF
$A2	PAICR	16	Port A interrupt control register	$0000
$A3	PAISR	4	Port A interrupt status register	$0
$A4	PBDR	11	Port B data register	$000
$A5	PBDDR	11	Port B data direction register	$7FF
$A6	PBICR	16	Port B interrupt control register	$0000
$A7	PBISR	4	Port B interrupt status register	$0
$A8	PCDR	6	Port C data register	$00
$A9	PCDDR	6	Port C data direction register	$3F
$AA	PDDR	6	Port D data register	$00
$AB	PDDDR	6	Port D data direction register	$3F

Note 1. Undefined at power-up, unmodified by reset.

2. Bits 11-0 are undefined, unmodfied by reset.

Table 16. Register Port Memory Map (continued)

Register Port Address	Register Name	Width (bits)	Description	Reset Value
$AC	PEDR	8	Port E data register	$00
$AD	PEDDR	8	Port E data direction register	$FF
$AE	PFDR	24	Port F data register	$000000
$AF	PFDDR	24	Port F data direction register	$FFFFFF
$B0	SCSR0	8	SPI 0 write control/read status register	$00
$B1	SSLVC0	16	SPI 0 slave configuration register	$0208
$B2	SWD0	16	SPI 0 write data register	$0000
$B3	SRD0	16	SPI 0 read data register	$0000
$B4	SBPR0	16	SPI 0 bit rate count preset register	$000F
$B5-$B7	Reserved	n/a	Reserved	n/a
$B8	SCSR1	8	SPI 1 write control/read status register	$00
$B9	SSLVC1	16	SPI 1 slave configuration register	$0208
$BA	SWD1	16	SPI 1 write data register	$0000
$BB	SRD1	16	SPI 1 read data register	$0000
$BC	SBPR1	16	SPI 1 bit rate count preset register	$000F
$BD-$BF	Reserved	n/a	Reserved	n/a
$C0	SCSR2	8	SPI 2 write control/read status register	$00
$C1	SSLVC2	16	SPI 2 slave configuration register	$0208
$C2	SWD2	16	SPI 2 write data register	$0000
$C3	SRD2	16	SPI 2 read data register	$0000
$C4	SBPR2	16	SPI 2 bit rate count preset register	$000F
$C5-$DF	Reserved	n/a	Reserved	n/a
$E0	Z0CFG	24	Zone 0 configuration register	$027F00
$E1	Z0TMR	32	Zone 0 timers configuration register	$00080004
$E2	Z1CFG	24	Zone 1 configuration register	$030000
$E3	Z1TMR	32	Zone 1 timers configuration register	$00010000
$E4	Z2CFG	24	Zone 2 configuration register	$030000
$E5	Z2TMR	32	Zone 2 timers configuration register	$00010000

Note 1. Undefined at power-up, unmodified by reset.

2. Bits 11-0 are undefined, unmodfied by reset.

Table 16. Register Port Memory Map (continued)

Register Port Address	Register Name	Width (bits)	Description	Reset Value
$E6	Z3CFG	24	Zone 3 configuration register	$030000
$E7	Z3TMR	32	Zone 3 timers configuration register	$00010000
$E8-$EF	Reserved	n/a	Reserved	n/a
$F0	IPL0	32	Interrupt priority vector assignment register 0	$76543210
$F1	IPL1	32	Interrupt priority vector assignment register 1	$FEDCBA98
$F2	IMASK	16	Interrupt mask register	$0000
$F3	ICFG0	16	Interrupt configuration register 0	$FFFF
$F4	ICFG1	16	Interrupt configuration register 1	$FFFF
$F5	ICLR	16	Interrupt clear register	$0000
$F6	IFLAG	16	Interrupt flag register	$0000
$F7-$FE	Reserved	n/a	Reserved	n/a
$FF	DVR	32	Device version register	$01020001

Note 1. Undefined at power-up, unmodified by reset.
2. Bits 11-0 are undefined, unmodfied by reset.

Data memory is divided into three areas: cached, direct mapped and Ethernet peripheral.

Table 17. Data Memory Map

Memory Address	Register Name	Width (bits)	Description	Reset Value
$000000-$7FFFFF	n/a	8/32	8 MB of cached memory area	n/a
$800000-$FFEFFF	n/a	8/32	direct mapped external memory	n/a
$FF0000	EMODER	32	eMAC mode register	$0000A800
$FF0004	EISOURCE	32	eMAC interrupt source register	$00000000
$FF0008	EIMASK	32	eMAC interrupt mask register	$00000000
$FF000C	EIPGT	32	eMAC b2b inter-packet gap register	$00000012
$FF0010	EIPGR1	32	eMAC non-b2b inter-packet gap register 0	$0000000C
$FF0014	EIPGR2	32	eMAC non-b2b inter-packet gap register 1	$00000012
$FF0018	EPKLEN	32	eMAC packet length register	$003C0600
$FF001C	ECOLLCFG	32	eMAC collision & retry configuration register	$000F003F
$FF0020	ERXBDNUM	32	eMAC transmit buffer descriptor number register	$00000080
$FF0024	ECTLMR	32	eMAC control module mode register	$00000000

Table 17. Data Memory Map (continued)

Memory Address	Register Name	Width (bits)	Description	Reset Value
$FF0028	EMIIMR	32	eMAC MII mode register	$00000064
$FF002C	EMIICR	32	eMAC MII command register	$00000000
$FF0030	EMIIADR	32	eMAC MII address register	$00000000
$FF0034	EMIITDR	32	eMAC MII transmit data register	$00000000
$FF0038	EMIIRDR	32	eMAC MII receive data register	$00000000
$FF003C	EMIISR	32	eMAC MII status register	$00000000
$FF0040	EMADR0	32	eMAC MAC address register 0	$00000000
$FF0044	EMADR1	32	eMAC MAC address register 1	$00000000
$FF0048	EHASH0	32	eMAC hash register 0	$00000000
$FF004C	EHASH1	32	eMAC hash register 1	$00000000
$FF0050-$FF03FF	Reserved	n/a	Reserved	n/a
$FF0400-$FF07FC	n/a	32	256-word single-port Ethernet buffer descriptor memory	n/a
$FF0800-$FF0FFF	n/a	32	Reserved	n/a
$FF1000-$FF13FF	n/a	32	1 kB dual-port Ethernet transmit buffer memory	n/a
$FF1400-$FF1FFF	n/a	32	3 kB dual-port Ethernet receive buffer memory	n/a
$FF2000-$FFFFFF	Reserved	n/a	Reserved	n/a

Tomahawk instruction memory is divided into two areas: direct mapped and cached.

Table 18. Program Memory Map

Memory Address	Width (bits)	Description
$000000-$7FFFFF	8	8 MB cached memory area
$800000-$FFFFFF	8	8 MB direct mapped external memory

6.0 Electrical Specifications

6.1 Absolute Maximum Ratings

Table 19. Absolute Maximum Ratings
V_{SS} = 0V(1)

Symbol	Parameter	Condition	Min	Max	Unit
V_{DD}	Supply Voltage	V_{DD} = 2.0V to 3.3V	V_{SS} - 0.5	4.0	V
V_I	Input Voltage(2)		V_{SS} - 0.5	V_{DD} + 0.5	V
		5.0V tolerant	V_{SS} - 0.5	5.5	
V_O	Output Voltage		V_{SS} - 0.5	V_{DD} + 0.5	V
T_{ST}	Storage Temperature		-55	+125	°C
T_J	Junction Temperature		-40	+125	°C
I_D	Supply Pin Current	One V_{DD} Pin		60	mA
		One V_{SS} Pin		60	mA
I_O(3)	Output Current	I_{OL} = 2.0 mA		±14	mA
		I_{OL} = 4.0 mA		±14	
		I_{OL} = 8.0 mA		±14	
		I_{OL} = 12 mA		±28	
		I_{OL} = 24 mA		±58	
		PCML output		20	
	Overshoot			V_{DD} + 1.0(4)	V
	Undershoot			V_{SS} - 1.0(4)	V

Note 1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions given in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Ratings for extended periods may affect device reliability.

2. Maximum of 1.1V between LVDSS differential inputs.

3. For a maximum of 1 ns.

4. For a maximum of 50 ns.

6.2 Recommended Operating Conditions

Table 20. Recommended Operating Conditions
V_{DD} = 3.3V, V_{SS} = 0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	Input High Voltage	3.3V CMOS	V_{DD} x 0.65		V_{DD} + 0.3	V
		3.3V Schmitt	V_{DD} x 0.80		V_{DD} + 0.3	
		5.0V-tolerant CMOS	V_{DD} x 0.65		5.25	
		5.0V-tolerant Schmitt	V_{DD} x 0.80		5.25	
V_{IL}	Input Low Voltage	3.3V/5.0V CMOS	V_{SS}		V_{DD} x 0.25	V
		3.3V/5.0V Schmitt	V_{SS}		V_{DD} x 0.20	
T_J	Junction Temperature				125	°C

Note 1. $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, memory is in standby mode.

2. When input buffers with pull-up or pull-down resistors are used, the I_{DDS} may be exceeded.
3. When input buffers with pull-up or pull-down resistors are used, I_{LI} or I_{LZ} may be exceeded.
4. Input buffers or bidirectional buffers may have pull-up or pull-down resistors.
5. Output shorted to V_{DD} or V_{SS}; maximum duration of one second on any pin.

6.3 DC Characteristics

Table 21. DC Characteristics
V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DDS}	Standby Supply Current(2)	Standby Mode 1(3)			200	µA
I_{CC}	Operating Supply Current	I/O C_{LOAD} = 60 pF		8.0	9.6	mA/ MHz
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	V_{DD} - 0.5		V_{DD}	V
		I_{OH} = -4.0 mA				
		I_{OH} = -8.0 mA				
		I_{OH} = -12.0 mA				
		I_{OH} = -24.0 mA				
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	V_{SS}		0.4	V
		I_{OL} = 4.0 mA				
		I_{OL} = 8.0 mA				
		I_{OL} = 12.0 mA				
		I_{OL} = 24.0 mA				
I_{LI}	Input Leakage Current(4)	$0 \le V_I \le V_{DD}$			±5	µA
I_{LZ}	Input Leakage Current (tri-state)(4)					µA
R_P	Input Pull-Up/Pull-Down Resistor(5)	Pull-down, $V_{IH} = V_{DD}$ Pull-up, V_{IL} = 0V	25	50	200	kΩ
I_{OS}	Output Short Circuit Current(6)	2.0 mA buffer			±30	mA
		4.0 mA buffer			±60	
		8.0 mA buffer			±120	
		12.0 mA buffer			±180	
		24.0 mA buffer			±360	

Note 1. $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, memory is in standby mode.

2. When input buffers with pull-up or pull-down resistors are used, the I_{DDS} may be exceeded.
3. PLLEN = low, $\overline{PULL}$ = high, and the device is not being clocked.
4. When input buffers with pull-up or pull-down resistors are used, I_{LI} or I_{LZ} may be exceeded.
5. Input buffers or bidirectional buffers may have pull-up or pull-down resistors.
6. Output shorted to V_{DD} or V_{SS}; maximum duration of one second any pin.

6.4 AC Characteristics

Table 22. AC Characteristics
Recommended operating conditions unless otherwise stated.

Symbol	Parameter	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time	Typ. x 0.72		Typ. x 1.65	ns
t_{PHL}					ns
t_{PZL}	Enable Time	Typ. x 0.72		Typ. x 1.65	ns
t_{PZH}					ns
t_{PLZ}	Disable Time	Typ. x 0.72		Typ. x 1.65	ns
t_{PHZ}					ns
Note 1. T_J = -40 to +125°C					

6.5 Capacitance

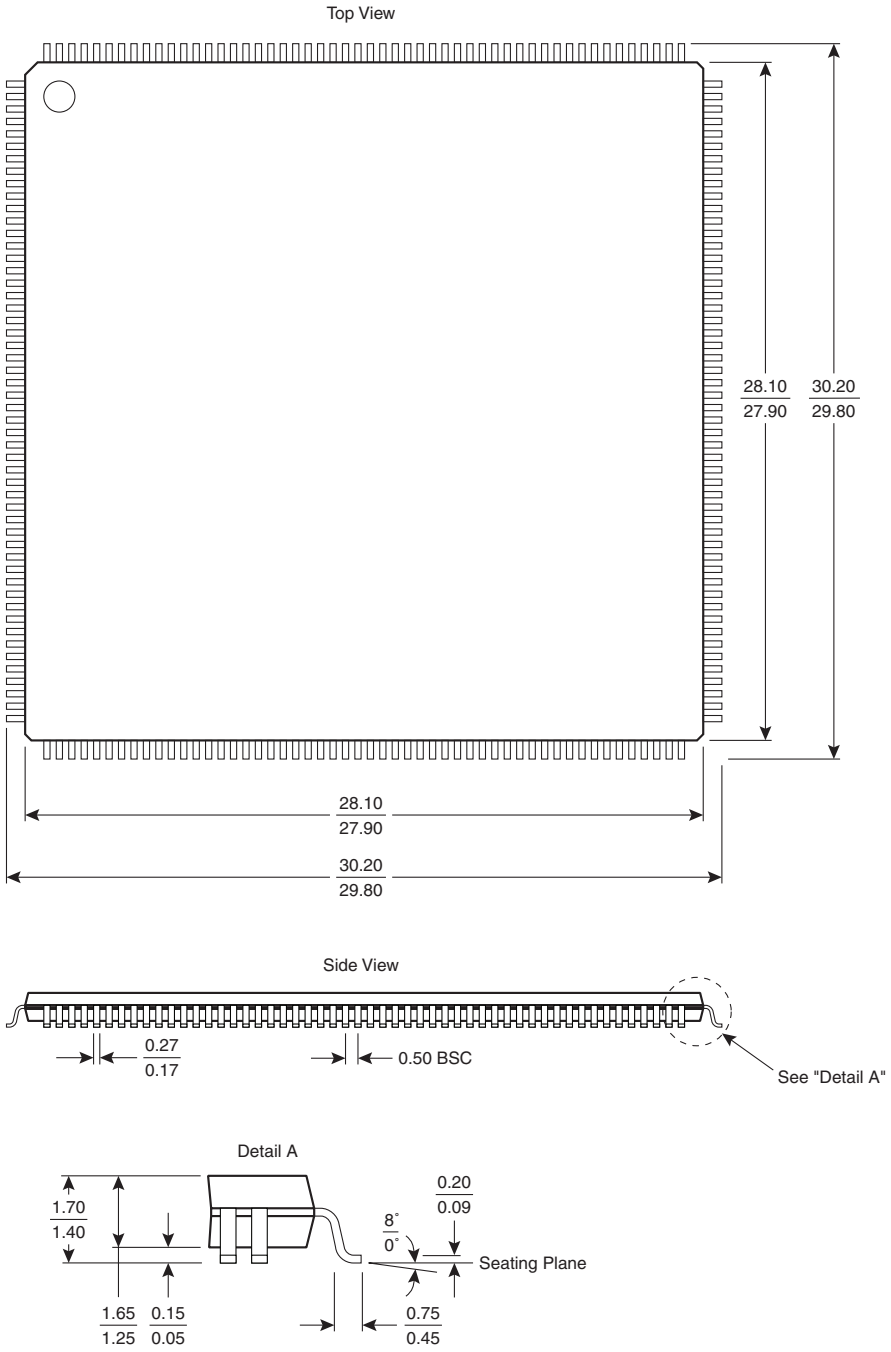
Table 23. Capacitance
T_A = 25°C, V_{DD} = V_I = 0V, f = 1 MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Input Pin Capacitance			16	pF
C_{OUT}(1)	Output Pin Capacitance			16	pF
C_{IO}(1)	I/O Pin Capacitance			16	pF
Note 1. I_{OL} = 2 mA, 4 mA, 8 mA, or 12 mA.					

7.0 Mechanical Specifications

The VS2000 is available in a 208-lead PQFP package.

Figure 4. 208Q, 30 x 30 mm, 208-Lead PQFP Package (dimensions in millimeters)



Note: Pin widths and thicknesses include plating.

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